On Silicon Carbide Thermal Oxidation

A. Benfdila [1,2,*] and K. Zekentes [3]
[1]*LMPDS, Fac. of Elect. & Comp. Eng., University M. Mammeri, Tizi-Ouzou Algeria*
[2]*ICTP-UNESCO-IAEA, Trieste, Italy*
[3]*MRG, IESL, FORTH, Vassilika Voutes, Heraklion Crete, Greece*

Thermal oxidation of silicon carbide (SiC) surface is based on the formation of either an active oxide (SiO_2) layer (Gate) for MOSFET fabrication or a passive (protective) oxide film for passivation and edge termination. The thermal oxidation kinetics and oxide-SiC interface are poorly understood in comparison to that of silicon. Furthermore, the quality of the SiO_2-SiC interface is also inferior to that of SiO_2/Si interface. Different thermal oxidation techniques are proposed to increase the efficiency as well as oxide and interface quality for manufacturing reliable power devices such as diodes and MOSFETs.

This paper deals with the recent developments in SiC technology and its thermal oxidation techniques aiming a better understanding of the electrical behavior of SiC power devices and seeking for more preferment devices.

1. Introduction

Silicon carbide (SiC) is an IV-IV compound that has distinguished characteristics and features as compared to other semiconductor compounds. It has excellent physical and electrical properties that allow fabrication of devices operating at significant higher temperature as compared to devices produced on silicon or GaAs. Silicon carbide has several advantageous properties such as chemical stability, higher thermal conductivity, as well as coefficient of thermal expansion and higher saturated electron velocity. A larger SiC bandgap (3 eV) leads to low leakage currents and higher breakdown voltages. Due to these electronic and physical properties, SiC has been chosen to fabricate high temperature, high frequency and high power electronic devices. In addition, it has been recognized as an ideal material for applications, where superior attributes such as hardness and stiffness, strength and oxidation resistance at elevated temperatures, as well as resistance to wear out and abrasion are of primary importance. There are various SiC polytypes having slightly different characteristics. The main polytypes are the 4H-SiC and 6H-SiC. The choice of a polytype relies on the SiC-SiO_2 interface and carrier mobility.

Fabrication of devices usually requires thick oxide layer growth during processing. Oxidation of SiC surface can be thermal or chemical deposition. In this work, we are concentrating on thermal oxidation, which is considered to be a breakthrough in SiC-MOS technology. Thermal oxidation is based on the formation of either an active oxide layer (Gate) or a passive (protective) SiO_2 film. Oxidation can be used to passivate the surface and to reduce the surface polishing damage produced by the etching of the oxide layer. The SiO_2/SiC interface is a critical element of many potential devices, including MOSFETs, charge-coupled devices (CCD), bipolar transistors (as a passivation layer), nonvolatile memories, and others.

The electrical quality of the thermally oxidized SiO_2/SiC-MOS interface depends on various factors. These are the surface preparation, oxidation ambience (wet or dry), oxidation temperature, substrate dopant type and concentration, orientation, substrate polytype, and post-oxidation annealing conditions. Generally, the growth rate of thermal oxidation on SiC, even at higher temperatures, is small compared to silicon. This does not allow adopting the selective oxidation, such as the local oxidation of silicon (LOCOS) used for device isolation in integrated circuits. The SiC oxidation rate depends on the SiC terminal face, i.e., oxidation on C-face is faster than on Si-face.

It is known [1] that the oxidation kinetics and oxide-SiC interface are poorly understood in comparison to that of silicon. The oxidation rate of SiC is lower than that of Si by a factor greater than 10. Furthermore, the quality of the SiO_2/SiC interface is also considerably inferior to that of SiO_2/Si interface. This problem causes low channel mobility in SiC-MOSFETs due to the high density

* benfdila@mail.ummto.dz; abenfdil@ictp.it

of interface states that exist in the band gap near the conduction band edge. Refinements [2-4] in cleaning and oxidation methods have improved the interface quality of SiO_2/SiC, but producing reliable devices will still require additional improvements.

There are different oxidation techniques [5-9] designed and proposed to improve the growth rate as well as the oxide and the oxide-interface quality. However, right now, there is no standard technique that gives the expected results in comparison to silicon oxidation.

A review of the state of the art of oxidation techniques and their impact on device performances is carried out after reviewing the oxidation models and processes.

2. Oxidation Modelling and Process

The growth process of SiO_2 layers on silicon carbide is similar to the growth on silicon. It can be carried out in a dry or wet atmosphere. There are two major striking differences between wet- and dry-grown oxides. These are the oxide growth rate and the oxide dielectric breakdown strength. However, the SiO_2-SiC interface and oxide quality are strictly depending on the oxidation type. For dry oxidation, the quality is high and hence the dielectric breakdown strength is also high, but the oxide layer is thinner. In contrast, the wet oxidation provides a bad interface and oxide quality, but thicker oxides.

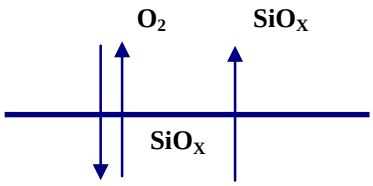
Wet oxidation consists of supplying a mixture of saturated H_2O vapour and oxygen to the oxidation environment (furnace). The growth rate in a wet ambience is much faster than in a dry ambiance (the parabolic rate constant for wet oxidation is about 25 times larger than that of dry oxidation at 1050°C). This is primarily due to a much higher solid solubility of H_2O in SiO_2 than O_2 in SiO_2, thus providing a much larger supply of oxidizing species to the SiC-surface. However, the dielectric breakdown strength of wet grown oxides is lower than that of dry grown oxides. This is mainly due to the slightly more porous nature of a wet oxide as compared to a dry oxide. Typical values of breakdown strength for wet-grown oxides on SiC are in the vicinity of 8 MV/cm. Moreover the interface states density is within the range of 10^{12}-10^{13} cm^{-2} for 6H SiC and even equal or greater than 10^{13} cm^{-2} for 4H-SiC.

Dry oxidation (sometimes called pyrogenic oxidation for temperatures greater than 1200°C) is simpler than wet oxidation. It is achieved by supplying an oxygen gas to the high temperature dry environment, typically 1000-1300°C. Dry oxidation results in a very good interface quality and high dielectric breakdown (11-12 MV/cm). However, it is a slow process as compared to wet oxidation and thus, the grown oxide layer is thinner. It is known that the density of interface states is within the ranges 10^{10}-10^{11} cm^{-2} for 6H-SiC and 10^{11}-10^{12} cm^{-2} for 4H-SiC.

In general, the oxidation procedure should be carried out following certain steps and schemes. The basic procedures are designed and developed by the CREE research. After a slow wafer load at around 800°C, a pre-oxidation in dry oxygen is first done at a temperature of about (800-900°C). Slowly, the ramp temperature is increased to the required value. It is desirable that SiC wafer surface faces the gas inlet. The oxidation should end by a dry oxidation followed by argon annealing under the same temperature. This annealing is meant for evacuation of all oxidation generated gases (mainly inside the oxide). A post-oxidation process (dry O_2 flow) is then achieved at 900 ^{O}C. Then, the temperature is decreased with the same rate as it was increased prior to the main oxidation step. This post-oxidation process is found to lower the interface sate density. As a last step, the temperature should be decreased at the same rate before the sample is removed. Under the above conditions, layers of 1 □m thickness are grown after 4 hours of dry oxidation in 1150 ^{O}C environment [10].

Mainly, oxidation follows two model schemes: active and passive as shown in Fig.1. Various analysis and modeling have been presented in [11], where the authors have modeled the theory and physics of the oxidation process. Fig. 1 describes these two oxidation processes. According to the oxidation model [12], there are three chemical reactions in the case of active SiC oxidation, i.e., SiC with SiO_2, SiC with O_2 and SiC with H_2O for the case of wet oxidation. All of them result in the formation of SiO and CO in the form of gas. The resultant chemical products, SiO and CO gases, react in the gas phase with oxygen (O_2) to produce CO_2 (gas) and SiO_2 (solid) is deposited on the oxide interface. An amount of CO is directly exhausted without reacting with O_2. However, the reverse phenomena occur especially at high temperature when SiC can react with SiO_2 and results in SiO and CO in gas forms. This reaction is very slow as compared to the first (direct one). The SiO and CO will be again reduced by O_2 to form SiO_2 and CO_2. The formation of the SiO material occurs always on the surface of the SiC and the deposition of SiO_2 is achieved in the oxidation

environment near the surface of the substrate on which it is deposited. This reaction generally occurs at higher temperature (say greater than 1150^{O}C). Oxide growth rate is known to be important compared to passive oxidation. In the case of passive oxidation, SiO_2 is directly produced from the first chemical reaction with O_2 in the oxidation environment. There are no intermediate reactions or products (like SiO). It occurs at temperature lesser than 1200^{O}C.



Active Oxidation

$Si^{(l)} \rightarrow Si^{(g)}$

$SiO_2^{(l)} \rightarrow Si^{(g)} + O_2$

$2\ Si_{(l)} + O_{2(g)} \rightarrow 2\ SiO_{(g)}$

$2\ SiO_2^{(l)} \rightarrow 2\ SiO^{(g)} + O_2$

$SiO_2^{(l)} + Si^{(l)} \rightarrow 2\ SiO^{(g)}$

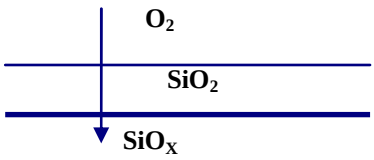
$Si^{(l)} + O_2 \rightarrow SiO_2^{(g)}$

$SiO_2^{(l)} \rightarrow SiO_2^{(g)}$

Environmental reactions:

$Si_{(l)} + H_2O_{(g)} \rightarrow SiO_{(g)} + H_{2(g)}$

$SiO_{2(s)} + H_{2(g)} \rightarrow SiO_{(g)} + H_2O_{(g)}$

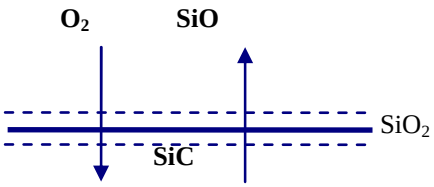


Passive Oxidation

$Si_{(l)} + 2\ H_2O_{(g)} \rightarrow SiO_{(l)} + H_{2(g)}$

$Si_{(l)} + O_{2(g)} \rightarrow SiO_{2(l)}$

$Si_{(l)} + 2\ H_2O_{(g)} \rightarrow SiO_{2(l)} + 2\ H_{2(g)}$



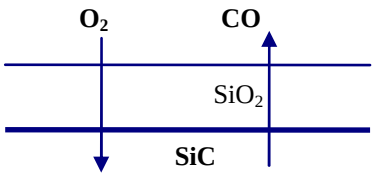
$SiC_{(s)} + O_{2(g)} \rightarrow SiO_{(g)} + CO_{(g)}$

Diffusion rate controlled reactions:

$SiC_{(s)} + 2\ SiO_{2(s)} \rightarrow 3\ SiO_{(g)} + CO_{(g)}$

Environmental reactions:

$SiC_{(s)} + 2\ H_2O_{(g)} \rightarrow SiO_{(g)} + CO_{(g)} + H_{2(g)}$



$SiC_{(s)} + n\ O_{2(g)} \rightarrow SiO_{2(l)} + CO_{x(g)}$

Fig.1: Oxidation Schemes Description, s: solid, g: gas, l: liquid, $SiO_{(g)}$: Intermediate material.

3. Oxidation Studied by Different Authors

The motivation behind many studies and investigations on SiC oxidation is the growth of SiO_2 films on SiC with the aim of obtaining a pure and thicker oxide layer that is free of electronic defects and supports higher fields. The SiC-MOSFET is expected to become available for the next-generation switching devices because it is faster than the bipolar transistor. Hence, 6H-SiC and 4H-SiC are currently used to fabricate high-temperature, high-power and high-frequency MOSFETs. However, the on-state resistance (R_{DSON}) of the SiC-MOSFET is much higher than the expected theoretical SiC values and the performance of SiC is not sufficiently tested. This can be attributed to several defects at the SiO_2/SiC interface, which leads to difficulties related to the current flow in the channel; i.e., low channel carrier mobility.

Silicon carbide oxidation is being improved through experimentation on MOS devices. For different oxidations and other processes, SiC-MOS capacitors are fabricated and characterized by their

I-V and C-V characteristics in order to know more about the oxide and oxide-SiC interface physics and technology.

A peer review on SiC oxides characterization is presented in [4]. It is known that typical oxide charge density (Q_{ot}) values are within the range 2.10^{11} - 8.10^{11} cm^{-2} and that of the interface state density (D_{it}) is around 5.10^{11} cm^{-2}.

It has been observed that oxide layer thickness versus temperature [10] curves saturate after a given temperature. The same thing is also observed in the case of oxide layer thickness versus time. Fig. 2 illustrates these behaviors with respect to time. It is clear that for higher temperatures, oxide thicknesses obtained for the same time duration are different. The higher temperature corresponds to thicker oxides. After a certain time, the oxidation process practically saturates. Golz et al. [13] proved that the time limit could be hundred hours and the thickness reached is 1.6 um. From Fig. 2, it can be seen that the growth rate increases linearly in a small time interval (less than 3 Hours) depending on the oxidation type (wet or dry). After the linear region, the saturation starts, but it is rather a drastic growth rate reduction (very slow) than a pure saturation (no variation with time). This fact may explain the result obtained in [13].

Hornetz [14] found that the oxidation faces some problems and limitations. The first layer on Si-faced SiC is a transitional layer of the form $Si_4C_{x-4}O_2$ and of average thickness 1 nm. This layer followed by a SiO_2 layer gives good interface quality compared to C-face. Indeed, for the C-faced SiC, the transitional layer is much thicker (several monolayers) and its exact composition is not well known.

Zetterling [15] showed that the square of the oxide layer thickness is linear with growth time up to 32 hours. This indicates that the growth rate does not saturate practically but experiences a drastic reduction.

Laukhe [16] found that the substrate quality plays an important role in the oxidation kinetics. Moreover, Muench and Pfaffender [17] noticed that the oxidation kinetics for the C-face depends on the substrate conductivity, i.e., on n-type substrate grows thicker oxide layer than on p-type substrate under the same conditions. SiC polytypes (6H, 4H and 3C) oxidizes differently. They demonstrated that the oxidation rate on Si-face increases when the degree of hexagonality decreases. It is independent on hexagonality in the case of C-face.

Shenoy [3] carried out the basic interface studies on 4H SiC-MOS structures and found the densities of interface states (D_{IT}) to be 10^{12} $eVcm^{-2}$. Utilizing rigorous cleaning and gentle loading procedures, he demonstrated a full order of

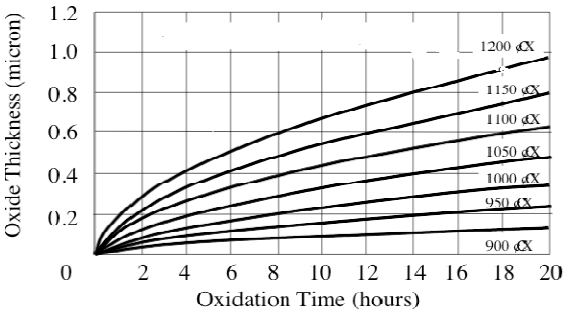


Fig.2: Effect of temperature and time on the oxide growth rates in the case of 4H-SiC Oxidation [after Cree Lab].

magnitude reduction in these states down to 10^{11} $eV^{-1}cm^{-2}$, i.e., a reduction of D_{IT} by a factor of 10. Lipkin et al. [18] made an annealing with a wet re-oxidation at 950°C and found that the D_{IT} density is reduced by a factor of 100, i.e., 10^{10} $eVcm^{-2}$. However, the interface state reduction did not led to carrier mobility increase in SiC-MOSFETs. Saks [19] explained later this fact by the presence of higher density of D_{IT} in the upper half bandgap (UHBIT), near conduction band, which is not affected by process optimization applicable to the lower half band D_{IT} (LHBIT). Unless other processes are introduced, the UHBIT remained unaffected.

Chung [20] and Lipkin [21] introduced the post-oxidation nitric oxide annealing, the first process that technologically reduced the UHBIT interface states. Annealing effect is illustrated in Fig.3. However, it has been observed that the underlying SiC substrate can be oxidized during the annealing process.

The research on SiC-MOS between 1992 and 1999 is devoted mainly to reduce D_{IT} in the lower half of the bandgap. However, in 1999, Das et al. [22] reported that DIT was much higher in the upper half of the bandgap, as determined from measurements on *n-type* MOS capacitors. They used alternative C-V LF-HF technique, where temperature is raised to about 300°C to achieve the characterization of the UHBIT. They observed that the effect is more pronounced in 4H-SiC than in 6H, because the bandgap in 4H is 250 meV wider than in 6H-SiC. Although D_{IT} is quite low in the lower half bandgap, it increases exponentially toward the conduction band.

Li et al. [23] originally reported improvements in the electrical performance of dry oxides on 6H-SiC annealed in nitric oxide (NO). Oxides grown on 4H-SiC, which experienced post oxidation anneals in NO, have D_{IT} density near the conduction band edge in n-4H-SiC comparable to DIT near the conduction band edge in 6H-SiC.

MacDonald [2] used the AC conductance and the HF-CV measurements at higher frequencies and focused mainly on the UHBIT in n-type SiC. This is achieved by the annealing, followed by a post-oxidation of the grown-oxide, and measuring under high temperature (350^{o}C). In addition, Yano [24] reported that the interface between SiO_2 and SiC could be improved by using a (0211) substrate orientation.

The presence of interface states resulting after native SiC oxidation and MOSFET study led to investigations on carrier mobility seen as a side effect of the oxidation process. It is known that the 4H polytype has higher bulk carrier mobility [25]. However, the reported channel mobilities for 4H *n*-channel inversion mode devices are substantially lower than for 6H-MOSFETs.

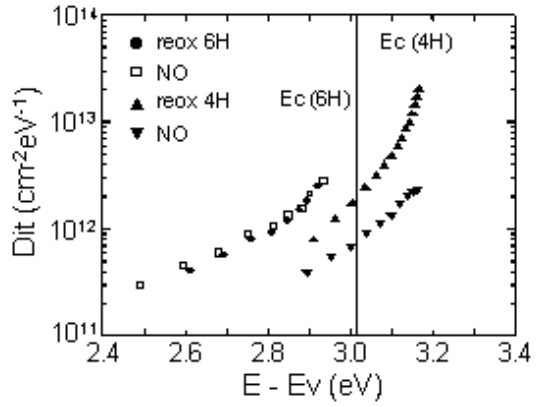


Fig.3: Interface state density for *n*-4H-SiC MOS capacitors before and after anneals in NO at 1175 ^{o}C for 2hr, after [19].

Schorner et al. [26] attributed the poorer performance of 4H devices to a large and broad interface state density located at approximately 2.9eV above the valence band edge in both polytypes. These interface states are within the band gap. Since 4H-SiC has a higher bandgap (~3.3eV) than that of 6H-SiC (~3eV) it is clear that their density is higher in the case of 4H-SiC. In both cases they act to reduce channel mobility through field termination, carrier trapping and Coulomb scattering.

Afanas'ev et al. [27] proposed that interface states in SiC/SiO_2 structures result from carbon clusters at the interface and defects in a near-interface sub-oxide that is produced when the oxidation process is terminated. The large interface trap density near the conduction band edge has been observed experimentally for both n-SiC and p-SiC.

Oxides grown on 4H-SiC that experienced post-oxidation annealing in NO at high temperatures showed [2] a great improvement of the effective channel mobility for inversion-mode SiC MOSFETs. S. Mitra [28] in a recent study found that AC conductance can give reliable results on both MOS capacitors and MOSFETs.

To improve the oxide quality other oxidation techniques are introduced. After the pyrogenic oxidation that consists mainly of going to higher temperatures (greater than 1250 ^{o}C), two other approaches are introduced. The first is the Atomic Oxygen Oxidation [5] and the second is the Nitrous Oxide Oxidation [6].

The Atomic oxygen technique uses a mixture of ozone (O_3) and oxygen O_2 in a heated quartz tube. Atomic oxygen is formed by the decomposition of ozone at high temperature to form O and O_2. It is found that the growth rate is increased and the interface quality is also improved. The Nitrous oxide oxidation originates from the properties of nitrogen annealing, where it is found that the channel mobility in MOS transistors is increased and the interface states density is decreased. It has been found [7, 8] that DIT is reduced and the SiC-SiO_2 quality is greatly improved for oxides grown in N_2O gas. The improvements get better as the temperature gets higher than 1250 ^{O}C. Moreover there is no need for nitridation as it is done in the oxidation process.

Recently, Lai et al. [9] investigated an improved dry-O_2 oxidation processing on n- and p-type 6H-SiC by adding a few mole percent of trichloroethylene (TCE) during dry O_2 oxidation. As a result, a large reduction of the interface-state density and oxide-charge density was obtained for both n- and p-type SiC MOS structures. Therefore, this probably provides a promising process for preparing excellent SiC-based MOSFETs with low interface-state density and high inversion-channel mobility.

As compared to conventional dry O_2 oxidation, the O_2 + TCE oxidation resulted in lower interface-state, border-trap and oxide-charge densities, and enhanced reliability. Moreover, they reported an increase in the oxidation rate in the O_2 + TCE ambient.

4. Conclusion

The reduction of interface-state density (D_{IT}) has been a major concern in SiC-based metal-oxide semiconductor (MOS) devices because it has a significant influence on the carrier mobility in the inversion channel. A suitable oxidation process is very important for obtaining a high-quality SiC/SiO_2 interface with low density of interface traps. It is believed that the high interface-state density near the conduction-band edge is mainly responsible for the low channel mobility. So far, many investigations are carried out to find a suitable way of achieving this goal.

It has been found that oxidation techniques are the major key for reducing the interfaces state density as well as increasing the maximum allowable gate field. Hence many oxidation techniques are proposed and implemented. In this study, it appears that the nitridation allows the reduction of D_{IT}. The modified conventional dry oxidation with TCE resulted in lower D_{IT} and higher oxidation rate.

Accordingly, the SiC-MOS future use is rather related to oxide growth technology. A suitable oxidation technique would result in faster and low-dimensional SiC-MOSFET, i.e., SiC integrated circuits.

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