Submicronic Holes Etching in the Cryogenic Process

N. Mekkakia Maaza[1,2], R. Dussart[1], T. Tillocher[1], C. Duluard[1], X. Mellhaoui[1],
P. Lefaucheux[1] and P. Ranson[1]
[1]*GREMI - Polytech'Orléans, Orléans Cedex 2, France*
[2]*Département d'Electronique, Faculté de Géni Electrique, USTO-MB, El Mnaouer, Oran, Algeria*

1. Introduction

The increasing development of Micro-Elecro-Mechanical Systems and the Lab-on-Chip introduces new challenges for deep silicon etching, where the defects such as undercut and crystallographic effect are not tolerated for these systems [1].

Two different kinds of deep etching process are used to realize such structures.

First, it is the Bosch process which uses a succession of etching and deposition steps at ambient temperature. In this process, etching is performed with SF_6 plasma and deposition with C_4F_8 plasma. After many steps of etching and deposition, deep and vertical etch profiles are achieved. Although, it is used often, the Bosh process presents many drawbacks such as scalloping effect, low etch rate, contamination, and process shift [1].

The second is the deep cryo-etching which is now a good alternative to the widely used Bosch process in many applications. It is based on SF_6/O_2 chemistry and the cooling of the substrate to cryogenic temperatures as low as –100°C. In this process the passivation layer SiO_xF_y is formed on the sidewalls, while silicon is etched at the hole bottom. It provides smooth profiles and high etch rates [2], [3]. However cryo-etching process is sensitive to temperature shifts, which can make etching or passivation dominate. In most cases, that leads to defects such as black silicon, undercut and bowing [4].

Crystallographic effect in cryo-etching process is characterized by Si (111) facets near the footprint of structures on Si(100) wafers as shown in Fig.1. However, this effect is absent on Si(111) wafers [5]. In this paper, the crystallographic effect and holes profiles are investigated by varying the process parameters such as chuck temperature and bias voltage.

2. Results and discussion

Samples with different apertures (from 2µm to 20µm) are etched during 3 minutes. During the experiment, the SF_6 flow rate, substrate temperature, rf power, bias voltage and pressure were kept constant at 350sccm, -85°C, 1500W, -90V and 9Pa, respectively. The O_2 flow rate decreases from 49 to 28sccm. Etch depth decreases quickly below a holes aperture of 8µm as shown in Fig. 2. A phenomenon usually labelled as aspect-ratio-dependent etching (ARDE) [6] or RIE lag [7] in which the etch rate decreases continuously during the etching process as the aspect ratio of the feature increases. In this case, the lag of etching rate for the 2 µm dimension compared to the 20 µm one is about 55%.

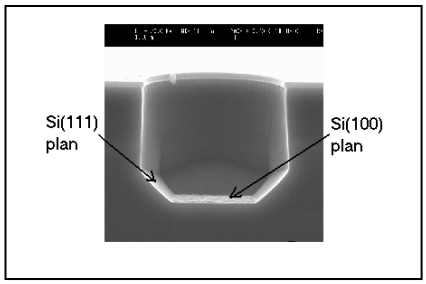

Fig.1: SEM images, formation of crystallographic facets at substrate temperature of –85°C.

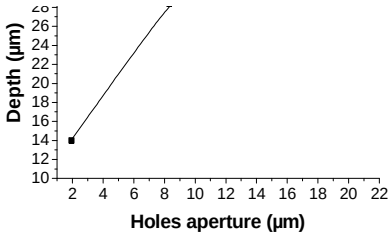

Fig.2: Etched depth vs hole's aperture.

For the same process conditions, Fig. 3 shows a strong dependence of sidewall taper and etch rate with respect to wafer temperature. The sidewall taper changes from positive to negative and crystal facets are formed at the bottom of the holes. Crystal facets are formed at the bottom of holes due to the stronger passivation of Si(111) as compared to Si(100).

Slopes can be adjusted by changing the wafer temperature, which could be of interest for designing specific MEMS.

For a substrate temperature below –100°C, the sticking coefficient of oxygen on silicon increases enhancing the passivation mechanism and so decreasing the etch rate [8].

Nevertheless, as shown in Fig. 3, a compromise has to be found so as to reach the specification: the high etch rate, correct profile slope. This compromise corresponds to a temperature set point of about –100°C.

For the same process conditions as mentioned above and at the temperature of –100°C, Fig. 4 shows holes etch rate as a function of bias voltage. From bias voltage of –50 to –110V, etch rates are constant and holes profiles slope are about 90°.

At –110V bias voltage, profiles became negative and the sidewall surface is exposed to a strong ion bombardment so that the passivation by oxygen radicals plays a minor role.

Crystal orientation dependent etching results in formation of facets near the footprint of structures on Si(100) wafers because the etch front tends to be limited by the Si(111) crystal planes. At –90V bias voltage, the crystallographic effect is less pronounced.

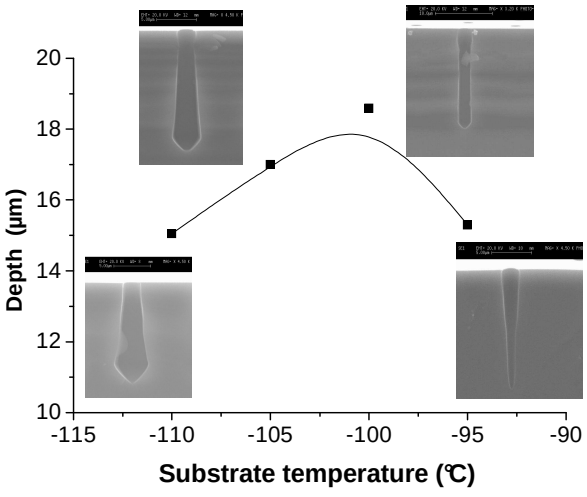

Fig.3: Etch depth and profiles vs substrate temperature.

3. Conclusion

We investigated a silicon cryo-etching process using SF6/O2 inductively coupled plasma. It is observed that the crystallographic effect and holes profile depend strongly on substrate temperature and bias voltage. At –100°C temperature and –90V bias voltage, etch rate is optimum about 6µm/min, holes profile slope is about 90° and crystallographic effect is less pronounced.

References

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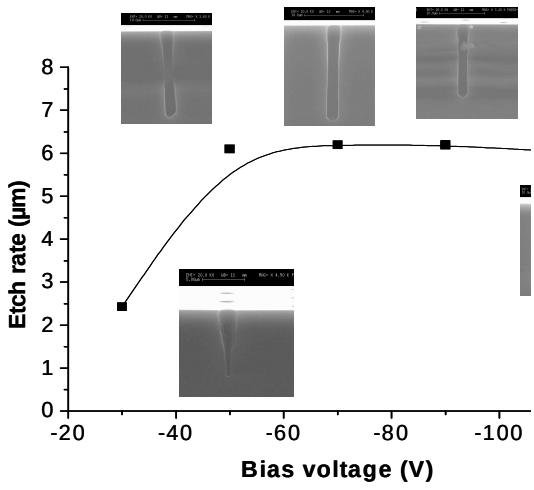

Fig.4: Etch rate and profiles vs Bias voltage.