

## On the Threshold Voltage Evolution for Submicronic MOS Transistors

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### 1. Introduction

The development of micro-electronics in the last few years is increasingly spectacular. This success mainly results from an increasingly thorough know-how and a technological master ship asset thanks to the new software. Transistor MOS is at the same time the principal actor and the vector of this technological development [1]. The constant reduction of the MOS transistors dimensions, notably the length of their channel and the oxide thickness, lead the apparition of parasitic phenomena [2]. This later corresponds to a modification of the threshold voltage and the preponderance of the "short channel effects" that damages the electric features of the MOS transistor [3].

In this paper, we expose firstly the main technological process of an ultimate MOS transistor. We consider, a  $0.35\mu\text{m}$  technology, simulated by the technological module "DIOS" of the ISE-TCAD (Integrated Systems Engineering – Technology Computer Aided Design) environment [4]. Then, we present the result of the electrical simulation. We use in this case the module "DESSIS" of the same software ISE-TCAD in order to observe the influence of the technological parameters and especially the effect of the oxide thickness (2.4 - 10nm), the length of the gate (0.18-  $0.5\mu\text{m}$ ) and the channel doping ( $3.7\text{e}17$ -  $3.5\text{e}18\text{cm}^{-3}$ ) on the behaviour of the MOS transistor, notably on the threshold voltage evolution  $V_T$ .

### 2. Main results

#### 2.1. Effect of the channel doping

We present the evolution of the threshold voltage according to the channel doping. We notice that for channel doping superior to  $8\text{e}17\text{ cm}^{-3}$ , the threshold voltage takes elevated values implying a large value of the gate voltage. However, it is very weak if channel doping varies between  $2.7\text{e}17\text{cm}^{-3}$  and  $7.18\text{e}17\text{cm}^{-3}$ . Therefore, the channel doping

becomes a key parameter to adjust the threshold voltage  $V_T$  (figure 1).

#### 2.2. Effect of the gate length

We observe the change of the threshold voltage according to the length of the channel. We note that for the channel lengths superior to  $0.5\mu\text{m}$ , the threshold voltage is independent of the channel length. At all times, the threshold voltage decreases strongly, when the channel lengths become inferior to  $0.2\mu\text{m}$  "short channel effect" (Fig. 2).

#### 2.3. Effect of the oxide thickness

We notice a strong dependence of the threshold voltage according to the oxide thickness. Indeed, the threshold voltage increases exponentially with the oxide thickness [5] (Fig. 3).

### 3. Conclusion

Our work relates to study of the impact of scaling on the performance of submicron n channel LDD MOSFET's. For the first time, the main technological process of a  $0.35\mu\text{m}$  MOSFET transistor is briefly presented using the module DIOS of the three-dimensional simulator ISE-TCAD. The main results of the electric simulation using the module DESSIS of the same software ISETCAD are then presented. Gate lengths of  $500\text{nm} > L_g > 180\text{nm}$ , and oxide thicknesses of 2.4nm and 10nm were considered. Channel doping, NA, was varied from  $3.5 \times 10^{17}/\text{cm}^3$  to  $3.5 \times 10^{18}/\text{cm}^3$ . The aim of our study is to highlight the contribution of the technological parameters (channel length, oxide thickness and channel doping) on the behaviour of the TMOS, in particular, on the threshold voltage evolution. It has been shown that during device optimization, the channel doping (NA) is increases as both the oxide thickness ( $T_{ox}$ ) and the channel lengths ( $L_g$ ) are scaled to maintain approximately the same device threshold voltage.

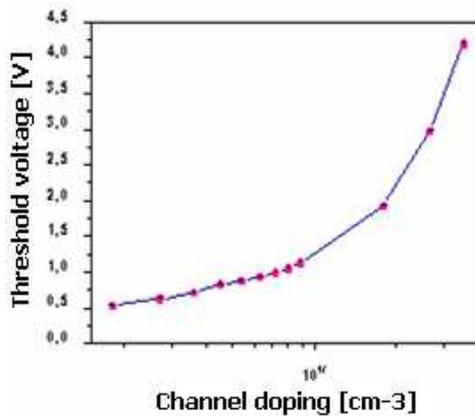


Fig.1: Evolution of the threshold voltage according to channel doping  $L_g=0.35\mu\text{m}$   $T_{ox}=3\text{nm}$

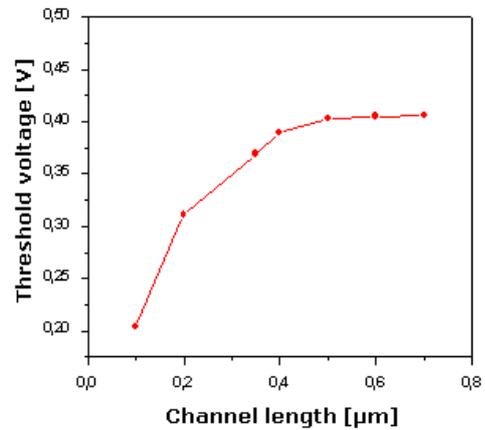


Fig.2: Evolution of the threshold voltage ( $V_{th}$ ) according to channel length  $T_{ox}=3\text{nm}$ .

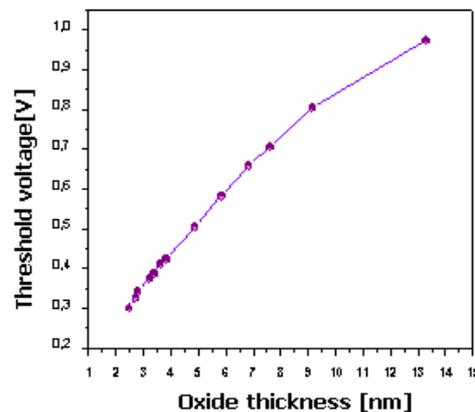


Fig.3: Evolution of the threshold voltage according to the gate oxide thickness  $L_g=0.35\mu\text{m}$ .

### References

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