Process Flow Mechanism for a Novel Trench Gate FLIMOSFET

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In this paper, we propose a possible process flow sequence to fabricate Trench Gate Floating Island (FLI) MOSFET (TG-FLIMOSFET) commercially by integrating multi-epitaxial process with trench gate technology. Power FLIMOSFET has been designed for improving the specific on-resistance (R_{on}) with respect to breakdown voltage (V_B) by decreasing the magnitude of the peak electric field distribution in the bulk by dividing into several sections. Deep trench gates have been used in the design of low on-resistance and for removing quasi-saturation effect in power MOSFETs. The TG-FLIMOSFET gives improved I-V characteristics in terms of quasi-saturation and reduced specific on-resistance.

1. Introduction

Recently, power MOSFET structures with P^+ floating islands such as FLIMOSFET [1-3] and oppositely doped buried regions (ODBR) MOSFET [4-5] has been designed for improving the specific on-resistance (R_{on}) versus breakdown voltage (V_B). The process flow mechanism required to fabricate FLIMOSFET structure using multi-epitaxial technology has been described in [5], which is less complex and less expensive than the super junction SJ device technology. However, FLIMOSFET devices also exhibit a current limiting effect at high current levels similar to that of a conventional power MOSFET despite of its having low specific on-resistance known as the quasi-saturation, which can be reduced by increasing the doping concentration of the drift region and by increasing the separation between adjacent MOS channels. However, these modifications cause the reduction in the forward blocking capability and also increase the total chip area of the device [6].

Deep trench gates have been used in the design of low on-resistance MOSFETs [7-10] and for removing quasi-saturation effect in power MOSFETs [11]. These two well established technologies (FLI/ODBR MOSFET and Trench gate) have been integrated with the help of device simulations [12] so as to form a Trench gate FLIMOSFET (TG-FLIMOSFET). Since the TG-FLIMOSFET gives improved I-V characteristics in terms of quasi-saturation and reduced specific on-resistance, in this paper, we propose a possible process flow required to fabricate such type of devices for the first time. The structure of the proposed trench-gate FLIMOSFET is schematically shown in Fig.1 along with its dimensions in microns designed using ISE-TCAD [13].

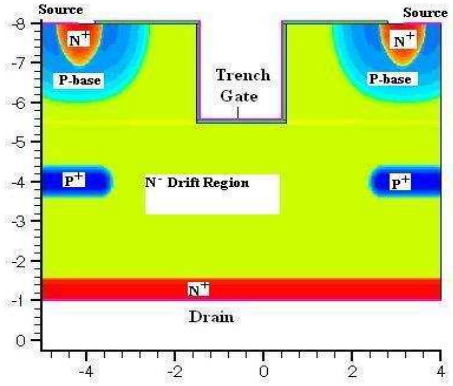

Fig.1: Cross-section of the proposed TG-FLIMOSFET. All dimensions are in microns.

2. Proposed process flow mechanism

The technology to fabricate FLI / ODBR MOSFET has been described recently using multi-epitaxial process [4-5]. Silicon trenches defined using reactive ion-etching (RIE) technique are being employed to fabricate the MOS gates for signal and power processing applications [9-10] Here, we propose a possible process flow sequence to fabricate TG-FLIMOSFET commercially by integrating multi-epitaxial process with trench gate technology. The process starts with a 0.002 to 0.004 Ω-cm, arsenic-doped <100> silicon substrate on top of which phosphorous-doped silicon drift region is to be epitaxially grown. The starting epitaxial region doping density N_{n-} can be kept within 1.0×10^{15} to 5.0×10^{15} cm^{-3} with a thickness of 15-25 μm. The P^+ floating layers are then incorporated into this drift region using buried multi-epitaxial growth process [5]. The buried P^+ floating layers thickness and width can be fixed within 1-3 μm. P^+ floating layers are formed in the

drift region by first masking the n- drift region by a oxide layer and then opening the windows for Boron implantation with doping density within 1.0×10^{17} to 5.0×10^{17}. Epitaxial growth is again carried out with the same doping density as in the starting epitaxial region. It should be noted that the epitaxial growth process is carried out at a substrate temperature of 1000 °C by chemical vapour deposition (CVD) using S_iH_4 gas. After these, P^+ floating layers are fabricated. The surface p-guard rings are required to be formed using boron ion-implantation followed by annealing.

Once the P^+ floating buried layers are fabricated along with the surface p-guard rings, a 0.5 μm thermal oxide layer is formed over the substrate. The windows are opened to pattern the trench gate using wet chemical etching of thermally grown SiO_2. To form the P-based region, Boron ions are implanted through the trench gate region and then annealed to form a junction depth of approximately 1.5 μm. Following a 0.25μm thick silicon nitride layer and a 0.25 μm thick TEOS oxide layer deposition by low pressure chemical vapour deposition (LPCVD), respectively, the TEOS oxide and silicon nitride layer are to be sequentially etched back by reactive ion etching (RIE) to form sidewall spacers.

Then by using the nitride/TEOS sidewall spacers, the thermal oxide as a masking layer, the rectangular trench with a depth of 2 to 4 μm and width of 0.6 to 2 μm has to be formed by RIE using a gas mixture of HBr and SiF_4. A sacrificial oxide is now grown and etched off to remove the damaged surface of the trenches and simultaneously to smooth the trench corners. Subsequently, a gate oxide has to thermally grown to thickness of 500-800A° at 1100°C in order to improve the uniformity of oxide thickness in trench bottom corners and sidewalls. The $POCl_3$- doped poly-silicon layer with the required thickness is to be deposited to refill trenches. After patterning of the poly-silicon gate electrode, $POCl_3$- doped poly-silicon layer is to be etched off by RIE to remove the poly-silicon layer on top of the surface. Followed by thermal oxidation to protect the poly-silicon layer during sidewall spacer removal, nitride/TEOS sidewall spacers are to be wet-etched using H_3PO_4 solution and then arsenic ions are implanted to form the N^+ source region of about 0.2 μm deep on each top side of the trench. In the end, a phosphorous-doped oxide is deposited over the entire wafer followed by heating the wafer to give a smooth surface topography. Contact windows are defined and etched followed by depositing and patterning a metal layer, such as aluminium to form ohmic contacts from source and drain regions. The entire sequence of the above process is being depicted in Figs. 2a-2g.

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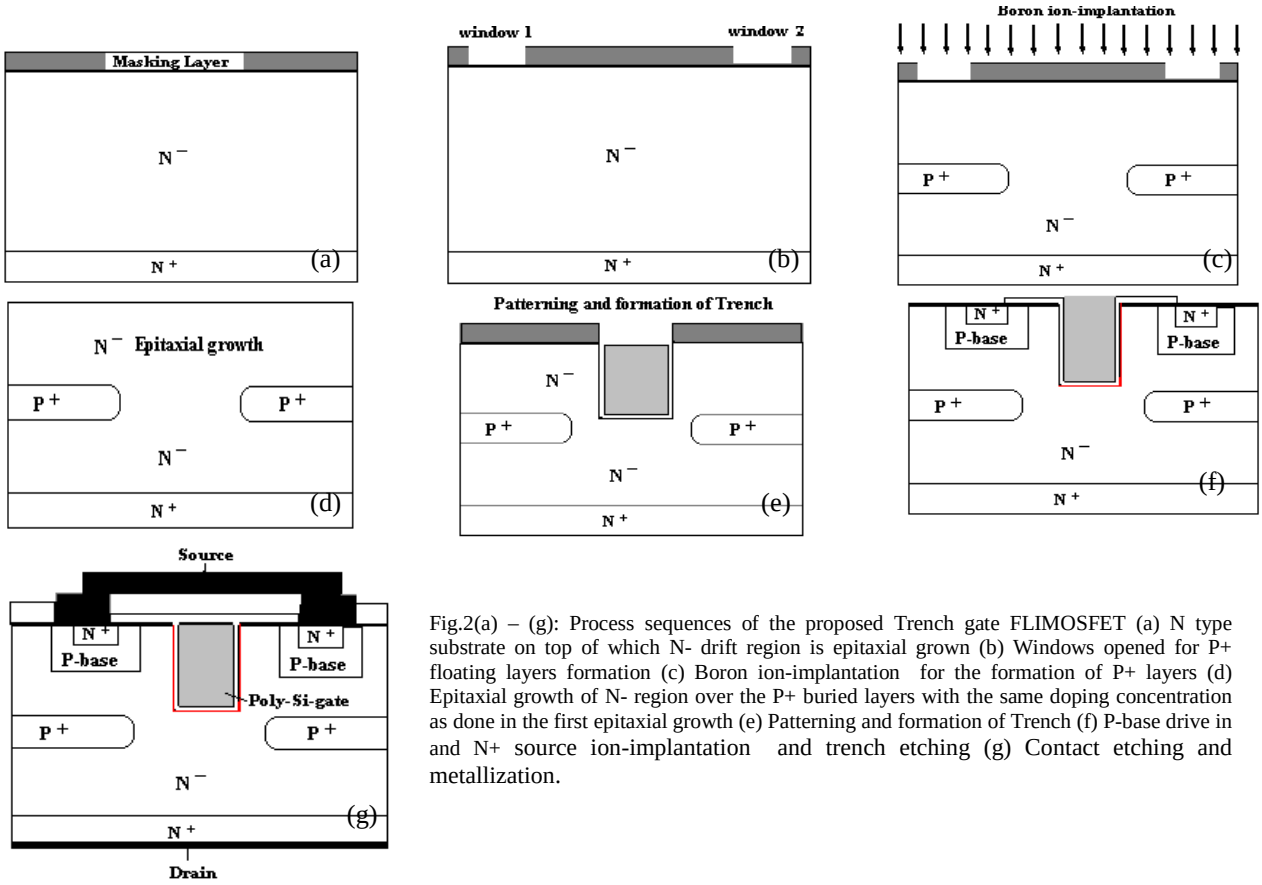

Fig.2(a) – (g): Process sequences of the proposed Trench gate FLIMOSFET (a) N type substrate on top of which N- drift region is epitaxial grown (b) Windows opened for P+ floating layers formation (c) Boron ion-implantation for the formation of P+ layers (d) Epitaxial growth of N- region over the P+ buried layers with the same doping concentration as done in the first epitaxial growth (e) Patterning and formation of Trench (f) P-base drive in and N+ source ion-implantation and trench etching (g) Contact etching and metallization.