Characterization of Slow Trap in MOS Capacitor

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Our study is devoted to an analysis of the defects in "slow states", which are supposed to be located in oxide close to the interface and which exchange carriers with the semiconductor by tunnel effect and in MOS capacities by using the Voltage Step technique. The aim is to clarify further results about this technique which were published earlier [1, 2, 3].

The evaluation of Tunnel depths, which play a very important role in the capture from the variation of the energy and the gate bias voltage, was made starting from the simulation of the potential of surface $\phi_s(V_g)$ using equations TMOS [4,5].

The MOS capacitor, used in the experiment was Ntype (substrate P), with an oxide thickness of 130Å, the flat-band voltage $V_{fb}=-1V$ and the threshold voltage was 0.4V. The voltage stepping and current response measurements were obtained using an HP4155A parameter analyser alone [6].

To obtain the current-voltage characteristics, the gate bias voltage was swept from inversion towards accumulation (from +3V to -3V), using a staircase waveform with a step voltage of 50mV per step, a hold time of 40sec, the set delay time was varied between 10ms and 1s and the measurement time was 65ms [6]. Following each measurement a delay of 2sec was allowed for the device to return to equilibrium before the next voltage step was applied.

As Fig. 1(a) shows, a positive peak current near the threshold voltage corresponds to the emission of the carriers and the recombination with the carriers of the substrate. However, a signal of low amplitude located around [-1, -0.25V] corresponds to the capture of the majority carriers (holes). Whereas, if the gate voltage is swapped from accumulation to the inversion (Fig. 1b), a negative peak current, which corresponds to the generation of the carriers (a signal of low amplitude) occurs in the surrounding of [-1V, 0.25V] corresponding to the emission of the minority carriers (electrons).

We measured also the current-voltage characteristics with different delay times, as can be seen from Fig. 2. It increases as the delay time reduces the peak of the current which can be explained as the reduction in the carriers.

Fig. 3 shows the slow trap concentration profiles extracted from the data points of Fig. 1. Finally, we have tried to analyse the slow trap concentration profiles in 03 dimensions (in-depth and in energy).

![Graph of Current-Voltage Characteristics](image-url)

Fig. 1 Current – Voltage characteristics of MOS Capacitor (a) showing positive current. Peaks when the voltage is swapped from inversion towards accumulation, and negative current peak when the stepping is in opposite direction.
References